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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,936	08/18/2003	Naoyuki Koizumi	CU-3332 RJS	4286

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EXAMINER	
DOTY, HEATHER ANNE	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,936	KOIZUMI, NAOYUKI	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *6-8* is/are withdrawn from consideration.

5)☒ Claim(s) *9* is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheldon (U.S. 3,642,597) in view of Wood et al. (U.S. 5,904,546).

Regarding claim 1, Sheldon teaches a method of fabricating a semiconductor chip from a semiconductor wafer having a first surface (top surface in Fig. 4) supporting a semiconductor element and a second surface opposite the first surface (bottom surface in Fig. 4), the method comprising the step of performing isotropic etching at least partially on a cutting portion of the semiconductor wafer from one or both of the first surface and the second surface, thereby forming a groove having a bowl-shaped cross section (Fig. 4; column 3, lines 33-44).

Sheldon further teaches separating the semiconductor wafer into individual semiconductor elements by cleavage along the bottom surface of the bowl-shaped groove by any conventional method (cleavage plane **420** in Fig. 4; column 8, lines 34-41), but does not expressly teach performing anisotropic etching on a bottom surface of the groove to separate the semiconductor wafer into individual semiconductor elements.

Wood et al. teaches a method of separating a semiconductor wafer into individual semiconductor elements by using anisotropic etching (Fig. 3; column 4, lines

21-53). This semiconductor dicing method is nonabrasive and does not form cracks or chips in the separated semiconductor elements, or adversely affect the electrical devices formed on the dice, as expressly taught by Wood et al. (column 2, lines 8-14).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Sheldon and Wood et al. by isotropically etching at least part of a cutting portion of a semiconductor wafer from one or both of the first and second surfaces, thereby forming a groove having a bowl-shaped cross section, and then separating the semiconductor wafer into individual semiconductor elements by dicing the wafer in the bowl-shaped grooves, as taught by Sheldon, using the anistropic etching method of wafer dicing taught by Wood et al. The motivation for doing so at the time of the invention would have been to avoid forming cracks or chips in the separated semiconductor elements, or adversely affecting the electrical devices formed on the dice, as expressly taught by Wood et al.

Regarding claim 2, Sheldon and Wood et al. together teach the method as claimed in claim 1. Sheldon further teaches forming a resist on the first surface to expose the cutting portion on the first surface, when the cutting portion is isotropically etched from the first surface (column 3, lines 22-31).

Regarding claim 4, Sheldon and Wood et al. together teach the method as claimed in claim 1. Sheldon further teaches forming a resist on the second surface to expose the cutting portion on the first surface, when the cutting portion is isotropically etched from the first surface (Fig. 4; column 3, lines 22-31).

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheldon (U.S. 3,642,597) in view of Wood et al. (U.S. 5,904,546) as applied to claims 1 and 4 above, and further in view of Bunch et al. (U.S. 2002/0145827).

Regarding claims 3 and 5, Sheldon and Wood et al. together teach the method of claims 3 and 5 as recited above in regard to claims 1 and 4, but they do not teach that the resist has rounded-off corners.

Bunch et al. teaches etching a silicon substrate using a resist with rounded-off corners to produce a surface with rounded edges (page 4, claim 20).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the rounded-off resist pattern taught by Bunch et al. as an etch mask for the isotropic etch taught by Sheldon and the anisotropic etch taught by Wood et al. to arrive at the invention as specified in claims 3 and 5. The motivation for doing so at the time of the invention would have been to achieve a surface with rounded edges, as expressly taught by Bunch et al.

Allowable Subject Matter

Claim 9 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: Prior art does not teach or suggest, in combination with the other claimed limitations, a method of dicing a semiconductor wafer using the process steps in the order as claimed in claim 9. Sheldon and Wood et al. together teach dicing a semiconductor wafer by making three grooves, one bowl-shaped groove on one surface, one bowl-shaped groove on the opposite surface, and a third groove coupled to

both bowl-shaped grooves, connecting them. But in their combined teaching it is the step of forming this third groove that actually separates the semiconductor elements. In claim 9, it is the step of forming the second bowl-shaped groove that separates the semiconductor elements.

Response to Arguments

Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

Tuan H. Nguyen
Primary Examiner